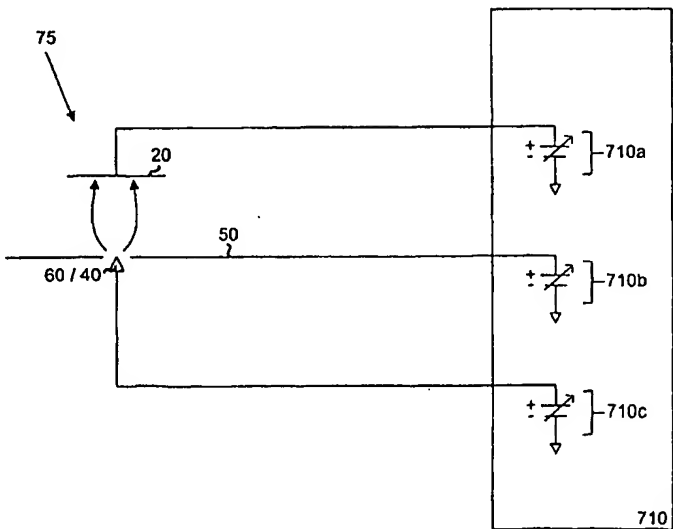




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G09G 3/10	A1	(11) International Publication Number: WO 00/13167 (43) International Publication Date: 9 March 2000 (09.03.00)
<p>(21) International Application Number: PCT/US99/15588</p> <p>(22) International Filing Date: 8 July 1999 (08.07.99)</p> <p>(30) Priority Data: 09/144,675 31 August 1998 (31.08.98) US</p> <p>(71) Applicant: CANDESCENT TECHNOLOGIES CORPORATION [US/US]; 6580 Via Del Oro, San Jose, CA 95153 (US).</p> <p>(72) Inventors: ELLOWAY, Donald, J.; 1109 Shady Dale Avenue, Campbell, CA 95008 (US). MORRIS, David, L.; 3644 El Grande Court, San Jose, CA 95132 (US). SCANNELL, William, J.; 1041 Ringwood, Menlo Park, CA 94025 (US). SPINDT, Christopher, J.; 115 Hillside Avenue, Menlo Park, CA 94025 (US).</p> <p>(74) Agents: GALLENSON, Mavis, S. et al.; Ladas & Parry, Suite 2100, 5670 Wilshire Boulevard, Los Angeles, CA 90036-5679 (US).</p>	<p>(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p>Published With international search report.</p>	
<p>(54) Title: METHOD AND APPARATUS FOR CONDITIONING A FIELD EMISSION DISPLAY DEVICE</p> <p>(57) Abstract</p> <p>700</p> <p>A method of removing contaminant particles in newly fabricated field emission displays. Contaminant particles are removed by a conditioning process which includes the steps of: a) driving an anode (20) of a field emission display (FED) to a predetermined voltage; b) slowly increasing an emission current of the FED after the anode has reached the predetermined voltage; and c) providing an ion-trapping device for catching the ions and particles knocked off, or otherwise released, by emitted electrons (40). By driving the anode to the predetermined voltage and by slowly increasing the emission current of the FED, contaminant particles are effectively removed without damaging the FED. A method of operating FEDs is also provided to prevent gate-to-emitter current during turn-on and turn-off, which comprises the steps of: a) enabling the anode display screen (20); and b) enabling the electron-emitters (40) after the anode display screen is enabled. By allowing sufficient time for the anode display screen to reach a predetermined voltage before the emitter is enabled, the emitted electrons (40) will be attracted to the anode (20).</p> 		

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

Method and Apparatus for Conditioning a Field Emission
Display Device

FIELD OF THE INVENTION

5 The present invention pertains to the field of flat panel display screens. More specifically, the present invention relates to the field of flat panel field emission display screens. There is disclosed in this description procedures and apparatus for turning-on and turning-off elements within a field emission display device.

BACKGROUND OF THE INVENTION

10 Flat panel field emission displays (FEDs), like standard cathode ray tube (CRT) displays, generate light by impinging high energy electrons on a picture element (pixel) of a phosphor screen. The excited phosphor then converts the electron energy into visible light. However, unlike conventional CRT displays which use a single or in some cases three electron beams to scan across the
15 phosphor screen in a raster pattern, FEDs use stationary electron beams for each color element of each pixel. This requires the distance from the electron source to the screen to be very small compared to the distance required for the scanning electron beams of the conventional CRTs. In addition, FEDs consume far less power than CRTs. These factors make FEDs ideal for portable
20 electronic products such as laptop computers, pocket-TVs, personal digital assistants, and portable electronic games.

- 2 -

One problem associated with the FEDs is that the FED vacuum tubes may contain a minute amount of contaminants which can become attached to the surfaces of the electron-emissive elements, faceplates, gate electrodes (including dielectric layer and metal layer) and spacer walls. These

5 contaminants may be knocked off when bombarded by electrons of sufficient energy. Thus, when an FED is switched on or switched off, there is a high probability that these contaminants may form small zones of high ionic pressure within the FED vacuum tube. In addition to the fact that the gate is positive with respect to the emitter, the presence of the high ionic pressure facilitates electron

10 emission from emitters to gate electrodes. The result is that some electrons may strike the gate electrodes rather than the display screen. This situation can lead to overheating of the gate electrodes. The emission to the gate electrodes can also affect the voltage differential between the emitters and the gate electrodes. In addition, as the electrons jump the gap between the electron-emissive

15 elements and the gate electrode, a luminous discharge of current may also be observed. Severe damage to the delicate electron-emitters may also result. Naturally, this phenomenon, generally known as "arcing," is highly undesirable.

Conventionally, one method of avoiding the arcing problem is by

20 manually scrubbing the FED vacuum tubes to remove contaminant material. However, it is difficult to remove all contaminants with that method. Further, the process of manual scrubbing is time-consuming and labor intensive, unnecessarily increasing the fabrication cost of FED screens.

- 3 -

Accordingly, the present invention provides an improved method of removing contaminant particles from the FED screen. The present invention also provides for an improved method of operating field emission displays to prevent gate-to-emitter currents during turn-on and turn-off. These and other advantages of the present invention not specifically described above will become clear within discussions of the present invention herein.

- 4 -

SUMMARY OF THE DISCLOSURE

The present invention provides for a method of removing contaminant material in newly fabricated field emission displays. According to one embodiment of the present invention, contaminant particles are removed by a conditioning process, which includes the steps of: a) driving an anode of a field emission display (FED) to a predetermined voltage; b) slowly increasing an emission current of the FED after the anode has reached the predetermined voltage; and c) providing an ion-trapping device for catching the ions and contaminants knocked off by emitted electrons. In this embodiment, by driving the anode to the predetermined voltage and by slowly increasing the emission current of the FED, contaminant particles are effectively removed without damaging the FED.

The present invention also provides for a method of operating FEDs to prevent gate-to-emitter current during turn-on and turn-off. In this embodiment, the method includes the steps of: a) enabling the anode display screen; and, b) enabling the electron-emitters a predetermined time after the anode display screen is enabled. In this embodiment, by allowing sufficient time for the anode display screen to reach a predetermined voltage before the emitter is enabled, the emitted electrons will be attracted to the anode. In this way, gate-to-emitter current is effectively eliminated when an FED is turned on. In the present embodiment, the anode display screen is enabled by applying a predetermined high voltage to the display screen, and the electron-emitters are enabled by

- 5 -

driving appropriate voltages to the gate electrodes and emitter electrodes of the FED.

In yet another embodiment of the present invention, the method of operating field emission displays to prevent gate-to-emitter current includes the steps of: a) disabling the emitters for a predetermined time; and, b) disabling the anode display screen after the electron-emitters are disabled. In this embodiment, by allowing sufficient time for the electron-emitters to be disabled before disabling the anode display screen, all remaining electrons will be attracted to the anode. In this way, gate-to-emitter current is eliminated during a turn-off sequence of the FED. In the present embodiment, the anode display screen is disabled by applying a ground voltage to the anode of the FED, and the electron-emitters are disabled by driving the gate electrodes and the emitter electrodes to the ground voltage.

15

Embodiments of the present invention include the above and further include a method of operating a field emission display, the method comprising the steps of: providing the field emission display with electron-emissive elements for emitting electrons, a gate electrode for controlling electron emission from the electron-emissive elements, and a display screen for collecting the electrons; enabling the display screen to establish a voltage differential between the display screen and the electron-emissive elements; and following enabling of the display screen, enabling the gate electrode by

20

- 6 -

delaying substantial electron emission from the electron-emissive elements until the voltage differential has been established to direct the electrons towards the display screen and to substantially prevent the electrons from striking the gate electrode.

5

Embodiments of the present invention further include a field emission display device comprising: a baseplate; a plurality of electron-emissive elements on the baseplate; a gate electrode on the baseplate for controlling electron emission from the electron-emissive elements; a display screen
10 spaced from the baseplate and configured for collecting electrons emitted from the electron-emissive elements to generate an image thereon; and a control circuit configured to control a flow of electrons to the electron-emissive elements, the control circuit allowing a voltage differential to be established between the display screen and the electron-emissive elements prior to
15 substantial electron emission from the electron-emissive elements to prevent substantial gate-to-emitter current during turn on of the field emission display device.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the present invention and, together with the description, serve to explain the principles of the invention.

5

Figure 1 is a cross section structural view of part of an exemplary flat panel FED screen that utilizes a gated field emitter situated at the intersection of a row line and a column line.

10

Figure 2 illustrates an exemplary FED screen in accordance with one embodiment of the present invention.

15

Figure 3 illustrates a voltage and current application technique for turning-on an FED device according to one embodiment of the present invention.

20

Figure 4 illustrates a flow diagram of the steps of an FED conditioning process according to one embodiment of the present invention.

Figure 5 illustrates a block diagram of a system for conditioning an FED according to one embodiment of the present invention.

- 8 -

Figure 6 illustrates a flow diagram of the steps of an FED turn-on procedure according to another embodiment of the present invention.

Figure 7 illustrates a flow diagram of the steps of an FED turn-off
5 procedure according to another embodiment of the present invention.

Figure 8 illustrates a voltage and current application technique for turning-on an FED device according to another embodiment of the present invention.

- 9 -

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the present embodiments of the invention, examples of which are illustrated in the accompanying drawings.

While the invention will be described in conjunction with the present

5 embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

Furthermore, in the following description, for purposes of explanation,

10 numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, upon reading this disclosure, that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are not described in detail in order to avoid obscuring
15 aspects of the present invention.

GENERAL DESCRIPTION OF FIELD EMISSION DISPLAYS

A general description of field emission displays is presented. Figure 1
20 illustrates a multi-layer structure 75 which is a cross-sectional view of a portion of an FED flat panel display. The multi-layer structure 75 contains a field-emission backplate structure 45, also called a baseplate structure, and an electron-receiving faceplate structure 70. An image is generated at faceplate

- 10 -

structure 70. Backplate structure 45 commonly consists of an electrically insulating backplate 65, an emitter (or cathode) electrode 60, an electrically insulating layer 55, a patterned gate electrode 50, and a conical electron-emissive element 40 situated in an aperture through insulating layer 55. One
5 type of electron-emissive element 40 is described in United States Patent Number 5,608,283, issued on March 4, 1997 to Twichell et al. and another type is described in United States Patent Number 5,607,335, issued on March 4, 1997 to Spindt et al., which are both incorporated herein by reference. The tip of the electron-emissive element 40 is exposed through a corresponding
10 opening in gate electrode 50. Emitter electrode 60 and electron-emissive element 40 together constitute a cathode of the illustrated portion 75 of the FED flat panel display. Faceplate structure 70 is formed with an electrically insulating faceplate 15, an anode 20, and a coating of phosphors 25. Electrons emitted from element 40 are received by phosphors portion 30. In one
15 embodiment, electron emissive element 40 includes a conical molybdenum tip. In other embodiments of the present invention, the anode 20 may be positioned over the phosphors 25, and the emitter 40 may include other geometrical shapes such as a filament.

20 The emission of electrons from the electron-emissive element 40 is controlled by applying a suitable voltage (V_G) to the gate electrode 50. Another voltage (V_E) is applied directly to the electron-emissive element 40 by way of the emitter electrode 60. Electron emission increases as the gate-to-emitter

- 11 -

voltage, e.g., V_G minus V_E , or V_{GE} , is increased. Directing the electrons to the phosphor 25 is performed by applying a high voltage (V_C) to the anode 20.

When a suitable gate-to-emitter voltage V_{GE} is applied, electrons are emitted from electron-emissive element 40 at various values of off-normal emission

5 angle theta 42. The emitted electrons follow non-linear (e.g., parabolic) trajectories indicated by lines 35 in Figure 1 and impact on a target portion 30 of the phosphors 25. Thus, V_G and V_E determine the magnitude of the emission current (I_C), while the anode voltage V_C controls the direction of the electron trajectories for a given electron emitted at a given angle.

10

Figure 2 illustrates a portion of an exemplary FED screen 100. The FED screen 100 is subdivided into an array of horizontally aligned rows and vertically aligned columns of pixels. The boundaries of a respective pixel 125 are indicated by dashed lines. Three separate row lines 230 are shown. Each

15 row line 230 is a row electrode for one of the rows of pixels in the array. In one embodiment, each row line 230 is coupled to the emitter cathodes of each emitter of the particular row associated with the electrode. A portion of one pixel row is indicated in Figure 2 and is situated between a pair of adjacent spacer walls 135. In other embodiments, spacer walls 135 need not be between each

20 row. And, in some displays, space walls 135 may not be present. A pixel row includes all of the pixels along one row line 230. Two or more pixels rows (and as much as 24-100 pixel rows), are generally located between each pair of adjacent spacer walls 135.

- 12 -

In color displays, each column of pixels has three column lines 250: (1) one for red; (2) a second for green; and (3) a third for blue. Likewise, each pixel column includes one of each phosphor stripes (red, green, blue), three stripes
5 total. In a monochrome display, each column contains only one stripe. In the present embodiment, each of the column lines 250 is coupled to the gate electrode of each emitter structure of the associated column. Further, in the present embodiment, the column lines 250 for coupling to column driver circuits (not shown) and the row lines 230 are for coupling to row driver circuits (not
10 shown).

In operation, the red, green and blue phosphor stripes are maintained at a high positive voltage relative to the voltage of the emitter-cathode 60/40. When one of the sets of electron-emission elements is suitably excited by
15 adjusting the voltage of the corresponding row lines 230 and column lines 250, elements 40 in that set emit electrons which are accelerated toward a target portion 30 of the phosphors in the corresponding color. The excited phosphors then emit light. During a screen frame refresh cycle (performed at a rate of approximately 60 Hz in one embodiment), only one row is active at a time and
20 the column lines are energized to illuminate the one row of pixels for the on-time period. This is performed sequentially in time, row by row, until all pixel rows have been illuminated to display the frame. The above FED configuration is described in more detail in the following United States Patents: US Patent

- 13 -

No. 5,541,473 issued on July 30, 1996 to Duboc, Jr. et al.; US Patent No. 5,559,389 issued on September 24, 1996 to Spindt et al.; US Patent No. 5,564,959 issued on October 15, 1996 to Spindt et al.; and US Patent No. 5,578,899 issued November 26, 1996 to Haven et al., which are incorporated
5 herein by reference.

FED CONDITIONING PROCEDURE ACCORDING TO
ONE EMBODIMENT OF THE PRESENT INVENTION

10 The present invention provides for a process of conditioning newly fabricated FEDs to remove contaminant particles contained therein. The conditioning process is performed before the FED device is used in normal operations, and is typically performed during manufacturing. During the conditioning process of the present invention, contaminants contained in the
15 vacuum tube of an FED are bombarded by a large amount of electrons. As a result of the bombardment, the contaminants will be knocked off and collected by a gas-trapping device (e.g., a getter). Because newly fabricated FEDs contain a large amount of contaminants, precautions steps must be taken to ensure that arcing does not occur during the conditioning process in
20 accordance with the present invention. To this end, according to the present invention, the conditioning process includes the step of driving the anode to a predetermined high voltage and the step of enabling the emission cathode thereafter to ensure that the electrons are pulled to the anode. In furtherance of

- 14 -

one embodiment of the present invention the emission current is slowly increased to the maximum value after the anode voltage has reached the predetermined high voltage.

5 Figure 3 illustrates a plot 300 showing the changes in anode voltage level and emission current level of a particular FED during the conditioning process of the present embodiment. Plot 301 illustrates the changes in anode voltage (V_c), and plot 302 illustrates the changes in emission current (I_c). Particularly, V_c is represented as a percentage of a maximum anode voltage
10 provided by the driver electronics. For instance, for a high voltage phosphor, a maximum anode voltage may be 3,000 volts. It should be noted that the maximum anode voltage may not be the normal operational voltage of the anode. For example, the normal operational voltage of the display screen may be 25% to 75% of the maximum anode voltage. I_c is represented as a
15 percentage of a maximum emission current provided by the driver circuits of the FED. Driver electronics and electronic equipment for providing high voltages and large currents to FEDs are well known in the art, and are therefore not discussed herein to avoid obscuring aspects of the present invention.

20 According to the present invention, plot 301 includes a voltage ramp segment 301a, a first level segment 301b, and a voltage drop segment 301c; and plot 302 includes a first current ramp segment 302a, a second current ramp segment 302b, a second level segment 302c, a third current ramp segment

- 15 -

302d, a third level segment 302e, and a current drop segment 302f. In the particular embodiment as shown, in the voltage ramp segment 301a, V_c increases from 0% to 100% of the maximum anode voltage over a period of approximately 5 minutes. Significantly, I_c remains at 0% as V_c increases to ensure that the electrons are pulled towards the display screen (anode) instead of the gate electrodes.

After V_c has reached 100% of the maximum anode voltage, V_c is maintained at that voltage level for roughly 25 minutes. Contemporaneously, I_c is slowly increased from 0% to 1% of the maximum emission current over approximately 10 minutes (first current ramp segment 302a). Thereafter, I_c is slowly increased to 50% of the maximum emission current over approximately 20 minutes (second current ramp segment 302b). I_c is then maintained at the 50% level for roughly 10 minutes (third level segment 302c). According to the present invention, I_c is increased at a slow rate to avoid the formation of high ionic pressure zones formed by desorption of the electron emitters. Desorbed molecules may form small zones of high ionic pressure, which may increase the risk of arcing. Thus, by slowly increasing the emission current, the occurrence of arcing is significantly reduced.

20

According to Figure 3, I_c is then maintained at a constant level for approximately 10 minutes (third level segment 302c) for "soaking" occur. Soaking refers to the process by which contaminant particles are removed by

- 16 -

gas-trapping devices. Gas-trapping devices, generally known as "getters," are used by the present invention at this stage of the conditioning process and are well known in the art.

5 In one embodiment, after the soaking period, I_c is then subsequently increased to 100% of its maximum level (third current ramp 302d) and, thereafter, remained at that level for approximately 2 hours (fourth level segment 302e). Contemporaneously, V_c is maintained at its maximum level. Thereafter, V_c and I_c are then subsequently brought back to 0% of their
10 respective maximum values. Significantly, as illustrated by segments 302f and 301c of Figure 3, I_c is turned off before V_c is turned off. In this way, it is ensured that all emitted electrons are pulled towards the display screen (anode) and that gate-to-emitter currents are prevented.

15 During the conditioning process of the present invention, any knocked off or otherwise released contaminants are collected by gas-trapping devices, otherwise known as "getters." Getters, as discussed above, are well known in the art. In the particular embodiment as illustrated in Figure 3, the total conditioning period is roughly six hours. After this conditioning period, most of
20 the contaminants would have been knocked off and collected by the getters, and the newly fabricated FED screen would be ready for normal operation.

- 17 -

Figure 4 is a flow diagram 400 illustrating steps of the FED conditioning process according to the present invention. To facilitate the discussion of the present invention, flow diagram 400 is described in conjunction with exemplary FED structure 75 illustrated in Figure 1. With reference now to Figures 1 and 4,

5 at step 410, the anode 20 of the FED is driven to a high voltage. It should be noted that, at step 410, the emission current (I_c) is maintained at 0% of the maximum level, and is therefore off. In one embodiment of the present invention, the voltage of the gate electrode 50 and the emitter-cathode 60/40 are maintained at ground. The anode voltage is driven to a high voltage while

10 maintaining an emission current at 0% to ensure that the electrons, once emitted, are pulled to the anode 20 rather than the gate electrode 50.

At step 420 of Figure 4, the emission current I_c is slowly increased to 1% of a maximum emission current provided by driver electronics of the FED. In

15 one particular embodiment of the present invention, step 420 takes roughly 5 minutes to accomplish. The slow ramp up ensures that localized zones of high ionic pressure will not be formed by desorption of the electron emitters. Further, in the present embodiment, the emission current I_c is proportional to the gate-to-emitter voltage (V_{GE}) as predicted by the Fowler-Nordheim theory. Thus, in the

20 present embodiment, the emission current I_c may be controlled by adjusting the gate-to-emitter voltage V_{GE} .

- 18 -

At step 430 of Figure 4, the emission current I_c is ramped up to approximately 50% of the maximum emission current provided by driver electronics of the FED. In one embodiment, step 430 takes roughly 10 minutes to accomplish. As in step 420, the slow ramp up allows ample time for
5 desorbed molecules to diffuse away, and ensures that localized zones of high ionic pressure are not formed.

At step 440 of Figure 4, emission current I_c and anode voltage V_c are maintained at 100% of their respective maximum values such that a large
10 amount of electrons will be emitted. The emitted electrons will bombard and knock off most loose contaminants unremoved by previous fabricating processes. The knocked off contaminants are subsequently trapped by ion-trapping devices such as the getters. As discussed above, getters are well known in the art, and are therefore not described herein to avoid obscuring
15 aspects of the invention.

At step 450, the emission current is brought to 0% of the maximum value. Subsequently, at step 460, the anode voltage is brought to 0% of its maximum value. It is important to note that emission current is turned-off prior to turning-
20 off the anode voltage such that all emitted electrons will be attracted to the anode. Thereafter, the conditioning process 400 ends.

- 19 -

Figure 5 is a block diagram 700 illustrating an apparatus for controlling the conditioning process according to one embodiment of the present invention. A simplified diagram of the FED 75 of Figure 1 is also illustrated. With reference to Figure 5, the apparatus includes a controller circuit 710 configured for

5 coupling to FED 75. Particularly, controller circuit 710 includes a first voltage control circuit 710a for providing an anode voltage to anode 20 of FED 75. Controller circuit 710 further includes a second voltage control circuit 710b for providing a gate voltage to gate electrode 50, and third voltage control circuit 710c for providing an emitter voltage to emitter cathode 60/40. It should be

10 appreciated that the controller circuit 710 is exemplary, and that many different implementations of the controller circuit 710 may also be used.

In operation, the voltage control circuits 710a-c provide various voltages to the anode 20, gate electrode 50 and emitter electrode 60/40 of the FED 75 to

15 provide for different voltages and emission current during the conditioning process of the present invention. In one embodiment of the present invention, the controller circuit 710 is a stand alone electronic equipment specially made for the present conditioning process to provide very high voltages. However, it should be appreciated that controller circuit 710 may also be implemented

20 within an FED to control the anode voltage and emission currents during turn-on and turn-off of the FED.

- 20 -

FED TURN-ON AND TURN-OFF PROCEDURES
OF THE PRESENT INVENTION

The present invention also provides for a method of operating a field
5 emission display to minimize the risk of arcing during power-on and power-off of
the FED unit. Particularly, according to one embodiment of the present
invention, the method of operating an FED includes the steps of: turning on the
anodic display screen of the FED, and, thereafter, turning on the emission
cathodes. According to another embodiment of the present invention, the
10 method of operating an FED to minimize the risk of arcing includes the steps of:
turning off the emission cathodes, and thereafter, turning-off the anodic display
screen. According to the present invention, the occurrence of arcing is
substantially reduced by following the aforementioned steps.

15 Figure 6 illustrates a flow diagram 500 of steps within an FED turn-on
procedure according to another embodiment of the present invention. In order
to facilitate the discussion of the present invention, flow diagram 500 is
described in conjunction with exemplary FED 75 of Figure 1. With reference
now to Figures 1 and 6, at step 510, when the FED 75 is switched on, the anode
20 20 is enabled. In the present embodiment, the anode is enabled by the
application of a predetermined threshold voltage (e.g. 300 V). Further, in the
present invention, the anode may be enabled by switching on a power supply
circuit (not shown) that supplies power to the anode 20. Power supplies for

- 21 -

FEDs are well known in the art, and any number of well know power supply devices can be used with the present invention.

At step 520, after the anode 20 of the FED 75 is enabled, and after the
5 anode has reached the predetermined threshold voltage, the emitter cathode
60/40 and the gate electrode 50 of the FED 75 are then enabled. In the present
invention, the emitter cathode 60/40 of the FED 75 is enabled a predetermined
period after the anode 20 has been enabled to direct the electrons towards the
anode 20 and to prevent the electrons from striking the gate electrode 50. In
10 one embodiment, the emitter cathode 60/40 and the gate electrode 50 may be
enabled by switching on the row and column driver circuits (not shown) of the
FED.

Figure 7 is a flow diagram 600 illustrating steps of an FED turn-off
15 procedure according to another embodiment of the present invention. In the
following, flow diagram 600 is discussed in conjunction with exemplary FED 75
of Figure 1. With reference now to Figure 1 and 7, at step 610, when the FED is
switched off, the emitter cathode 60/40 and the gate electrode 50 of the FED 75
are disabled. Contemporaneously, the anode 20 remains at a high voltage.
20 Further, in one embodiment, the emitter cathode 60/40 and gate electrode 50
are disabled by setting the row voltages and column voltages respectively
provided by row drivers and column drivers (not shown) to a ground potential.

- 22 -

At step 620, after the emitter cathode 60/40 and the gate electrode 50 are disabled, the anode 20 of the FED is disabled. According to the present invention, step 620 is performed after step 610 in order to ensure that all electrons emitted from emission cathodes will be attracted to the anodic display screen. In one embodiment, the anode 20 is disabled by switching off the power supply circuit (not shown) that supplies power to the anode 20. In this way, the occurrence of arcing in FEDs is minimized.

FED CONDITIONING PROCESS ACCORDING TO ANOTHER EMBODIMENT OF THE INVENTION

Figure 8 is a plot 800 illustrating a voltage and current application technique for conditioning a particular FED device according to another embodiment of the present invention. Plot 801 illustrates the changes in anode voltage (V_c), and plot 802 illustrates the changes in emission current (I_c). Particularly, V_c is represented as a percentage of a maximum anode voltage provided by the driver electronics. I_c is represented as a percentage of a maximum emission current provided by the driver circuits of the FED.

According to the present invention, plot 801 includes voltage ramp segments 810a-d, constant voltage segments 820a-f, voltage drop segments 830a-c; and plot 302 includes current ramp segments 840a-e, constant current segments 850a-e, and current drop segments 860a-c. In the particular

- 23 -

embodiment as shown, in the voltage ramp segment 810a, V_c increases from 0% to 50% of the maximum anode voltage over a period of approximately 10 minutes. Significantly, I_c remains at 0% as V_c increases to ensure that the electrons are pulled towards the display screen (anode) instead of the gate electrodes.

After V_c has reached 50% of the maximum anode voltage, V_c is maintained at that voltage level for roughly 30 minutes (constant voltage segment 820a). Contemporaneously, I_c is slowly increased from 0% to 1% of the maximum emission current over approximately 10 minutes (current ramp segment 840a). Thereafter, I_c is slowly increased to 50% of the maximum emission current over approximately 10 minutes (current ramp segment 840b). I_c is then maintained at the 50% level for roughly 10 minutes (constant current segment 850a). According to the present invention, I_c is increased at a slow rate to avoid the formation of high ionic pressure zones formed by desorption of the electron emitters. Desorbed molecules may form small zones of high ionic pressure, which may increase the risk of arcing. By slowly increasing the emission current, ample time is allowed for the desorbed molecules may diffuse to gas-trapping devices (e.g., getters). In this way, occurrence of arcing is significantly reduced.

According to Figure 8, V_c is reduced from 50% to 20% level (voltage drop segment 830a) and is maintained at the 20% level for roughly 30 minutes

- 24 -

(constant voltage segment 820b). After V_c has reached the 20% level, I_c is slowly ramped up to the 100% level (current ramp segment 840c). It should be noted that the 20% level is selected such that the anode voltage is close to a minimum threshold level for the anode of the FED to attract the emitted
5 electrons. I_c is then maintained at a constant level for approximately 20 minutes (constant current segment 820b) for "soaking" occur.

In the present embodiment, I_c is then subsequently decreased to 50% of its maximum level (current drop segment 860a) and, thereafter, remained at that
10 level for approximately 20 minutes (constant current segment 850c). After I_c has reached the 50% level, V_c is increased to the 50% level (voltage ramp segment 810b) and is maintained at that level for 20 minutes (constant current level 820c). Thereafter, I_c is turned-off to 0% of its maximum value (current drop segment 860b).

15

After I_c is turned off, V_c is slowly ramped up to 100% of its maximum level over a period of approximately 2.5 hours (voltage ramp segment 810c), and is maintained at the maximum level for approximately 1 hour (constant voltage segment 820d). Thereafter, V_c is decreased to the 50% level (voltage drop
20 segment 830b), and is maintained at that level for approximately 20 minutes (constant voltage segment 820e). I_c is slowly increased from 0% to the 50% level (current ramp 840d) when V_c is at 50% level. V_c and I_c are then subsequently driven to 100% of their respective maximum values (voltage ramp

- 25 -

segment 810d and current ramp segment 840e), and are maintained at those levels for approximately 1.5 hours (constant voltage segment 820f and constant current segment 850e). Thereafter, V_c and I_c are brought back to 0% (voltage drop segment 830c and current drop segment 860c).

5

Significantly, as illustrated by segments 810d and 840e of Figure 8, I_c is driven to the maximum value after V_c is driven to the maximum value, and I_c is turned off before V_c is turned off. In this way, it is ensured that all emitted electrons are pulled towards the display screen (anode) and that gate-to-emitter
10 currents are prevented.

The present invention, a method of operating an FED to minimize the occurrence of arcing in FED has thus been disclosed. It should be appreciated that electronic circuits for implementing the present invention, particularly the
15 circuits for delaying the activation of the emissive cathode until a threshold voltage potential has been established, are well known. For instance, it should be apparent to those of ordinary skill in the art, upon reading the present disclosure, that a control circuit responsive to electronic control signals may be used to sense the anode voltage and to turn on the power supply to the row and
20 column drivers after the anode voltage has reached a threshold value. It should also be appreciated that, while the present invention has been described in particular embodiments, the present invention should not be construed as

- 26 -

limited by such embodiments, but rather construed according to the below claims.

- 27 -

CLAIMS:

5

What is claimed is:

1. A method of conditioning a field emission display, the method comprising the steps of:

- 10 a) providing the field emission display with electron-emissive elements for emitting electrons, a gate electrode for controlling electron emission from the electron-emissive elements, and a display screen for collecting the electrons;
- b) enabling the display screen to establish a voltage differential
- 15 between the display screen and the electron-emissive elements;
- c) following enabling of the display screen, enabling the gate electrode by delaying substantial electron emission from the electron-emissive elements until the voltage differential has been established to direct the electrons towards the display screen and to substantially prevent the electrons
- 20 from striking the gate electrode; and
- d) following enabling the gate electrode, lowering a voltage of the display screen to a predetermined level;

- 28 -

e) following lowering the voltage of the display screen, increasing a voltage of the gate electrode to increase an emission current; and

f) repeating the steps (d) and (e) until a threshold voltage at the display screen is reached.

5

2. The method as claimed in Claim 1 wherein the display screen comprises an anode.

3. The method as claimed in Claim 1 wherein the step (b) further comprises
10 the step of driving a predetermined anode voltage to the display screen.

4. The method as claimed in Claim 1 wherein the step (c) further comprises the step of driving a predetermined gate voltage to the gate electrode.

15 5. The method as claimed in Claim 1 wherein the electron-emissive elements comprise conical electron emitters.

6. The method as claimed in Claim 5 wherein the conical electron emitters each comprises a molybdenum tip.

20

7. The method as claimed in Claim 1 further comprising the steps of:

g) preventing further electron emission by disabling the gate electrode; and

- 29 -

h) following disabling the gate electrode, disabling the display screen to prevent the electrons from striking the gate electrode.

8. A method of conditioning a field emission display screen, the field
5 emission display screen having an anode, a gate electrode and an emitter cathode, the method comprising the steps of:
driving the anode of the field emission display to a threshold voltage; and
controlling an emission current of the field emission display to increase
from a substantially zero level to a maximum level, wherein the step of
10 controlling is performed after the step of driving to avoid forming electric arcs in
the field emission display screen when the field emission display is initially
turned on.

9. The method according to Claim 8 wherein the emission current is
15 controlled by applying appropriate voltages to the gate electrode and the
emitter cathode.

10. The method according to Claim 8 further comprising the steps of:
decreasing the emission current of the field emission display from the
20 maximum level to the substantially zero level;
disabling the anode of the field emission display, wherein the step of
decreasing is performed prior to the step of disabling to direct the electrons

- 30 -

towards the anode and to prevent the electrons from striking the gate electrode when the field emission display is turned off.

11. The method according to Claim 10 further comprising the steps of:
5 maintaining the anode at the predetermined voltage; and
 maintaining the emission current at the maximum level for a
predetermined period in order to knock off contaminants contained in the field
emission display screen.
- 10 12. The method according to Claim 10 further comprising the step of
providing a gas-trapping device to trap the contaminants.
13. The method according to Claim 8 wherein the emitter cathode is coupled
to a plurality of conical electron emitters.
- 15 14. The method as claimed in Claim 13 wherein the conical electron emitters
each comprises a molybdenum tip.
15. The method according to Claim 8 wherein the step of controlling
20 comprises the step of slowly increasing the emission current from a zero level to
approximately 1% of the maximum level over a period of at least 10 minutes.

- 31 -

16. The method according to Claim 12 wherein the step of controlling further comprises the step of slowly increasing the emission current from the 1% level to approximately 50% of the maximum level over a period of approximately 20 minutes.

5

17. An apparatus for conditioning a field emission display, the apparatus comprising:

means for providing the field emission display with electron-emissive elements for emitting electrons, a gate electrode for controlling electron
10 emission from the electron-emissive elements, and a display screen for collecting the electrons;

means for enabling the display screen to establish a voltage differential between the display screen and the electron-emissive elements;

means for enabling the gate electrode following enabling of the display
15 screen by delaying substantial electron emission from the electron-emissive elements until the voltage differential has been established to direct the electrons towards the display screen and to substantially prevent the electrons from striking the gate electrode;

means for lowering a voltage of the display screen to a predetermined
20 level following enabling the gate electrode;

means for increasing a voltage of the gate electrode to increase an emission current following lowering the voltage of the display screen; and

- 32 -

means for alternately lowering the voltage of the display screen and increasing the emission current until a threshold voltage at the display screen is reached.

5 18. The apparatus as claimed in Claim 17 wherein the display screen comprises an anode.

19. The apparatus as claimed in Claim 17 wherein means for enabling the display screen further comprises means for driving a predetermined anode
10 voltage to the display screen.

20. The apparatus as claimed in Claim 17 wherein means for the gate electrode further comprises the step of driving a predetermined gate voltage to the gate electrode.

15

21. The apparatus as claimed in Claim 17 wherein the electron-emissive elements comprise conical electron emitters.

22. The apparatus as claimed in Claim 21 wherein the conical electron
20 emitters each comprises a molybdenum tip.

23. The apparatus as claimed in Claim 17 further comprising:

means for preventing further electron emission by disabling the gate electrode; and
means for disabling the display screen to prevent the electrons from striking the gate electrode following disabling the gate electrode.

24. A conditioning process comprised of the steps of:
- a) driving an anode of a field emission display (FED) to a predetermined voltage;
 - b) increasing an emission current of the FED after the anode has reached the predetermined voltage; and
 - c) providing an ion-trapping device for catching the released ions and particles.
25. A method to prevent gate to emitter current comprising the steps of:
- a) enabling the anode display screen; and
 - b) enabling the electron-emitters after the anode screen is enabled.

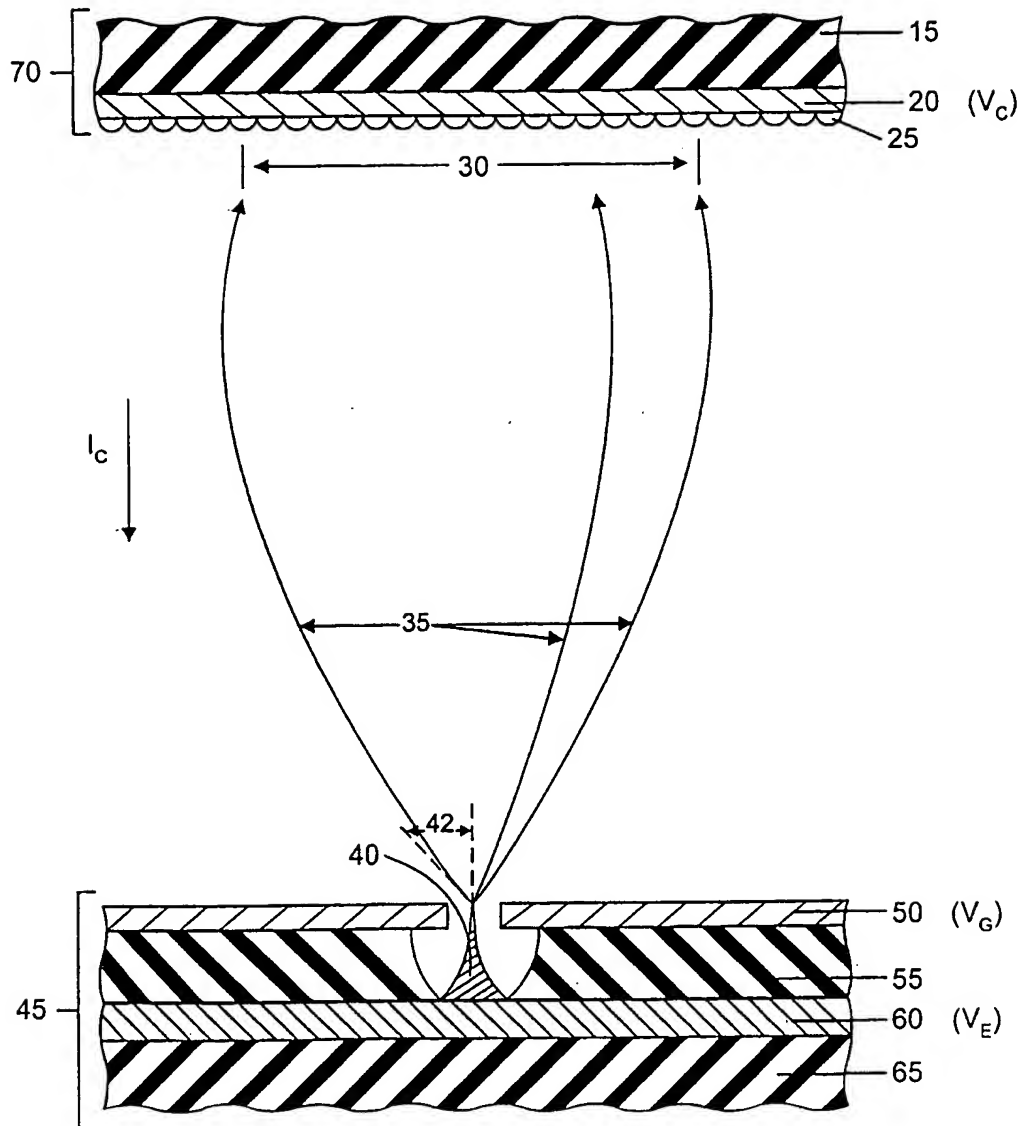
75

FIG. 1

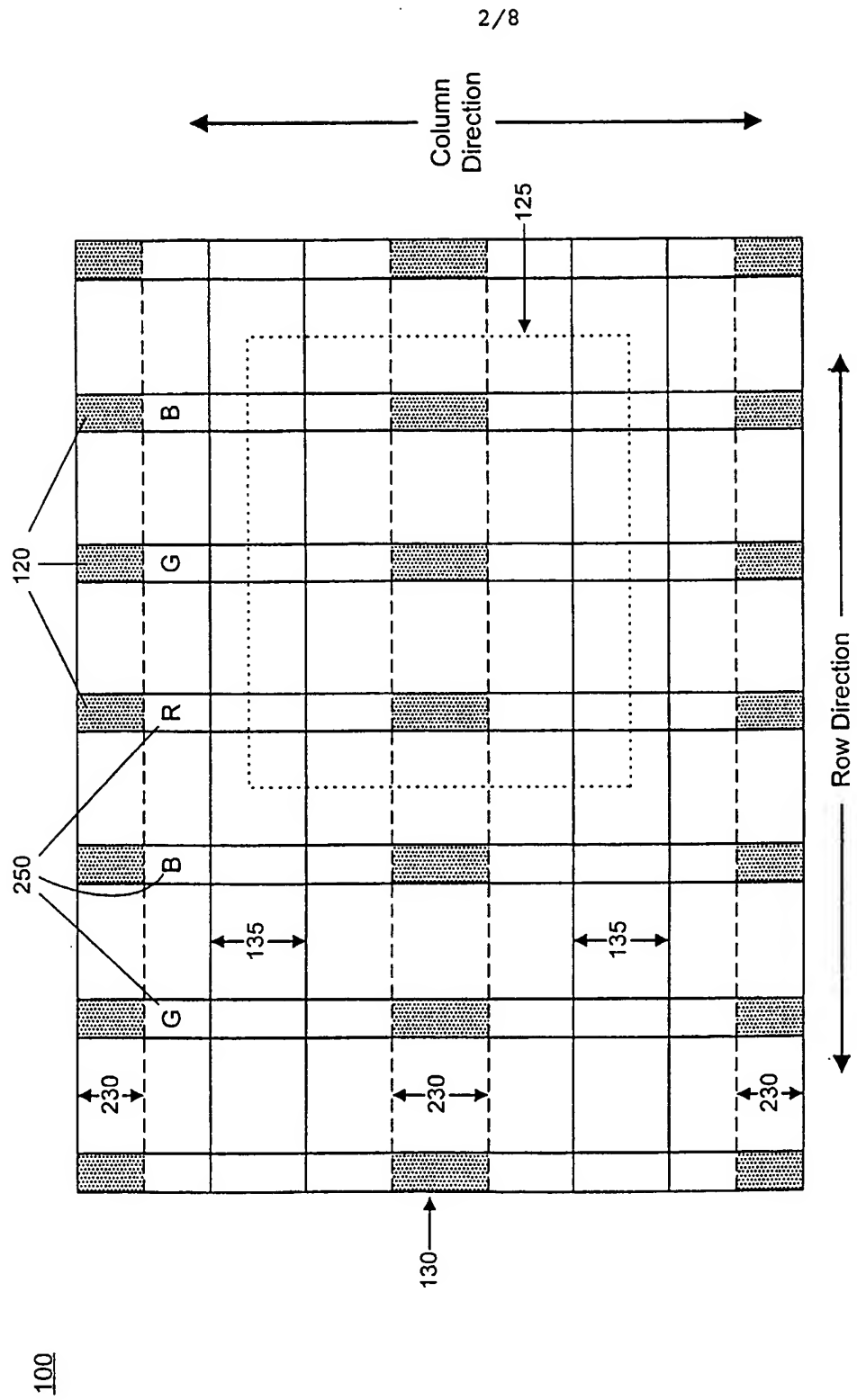


FIG. 2

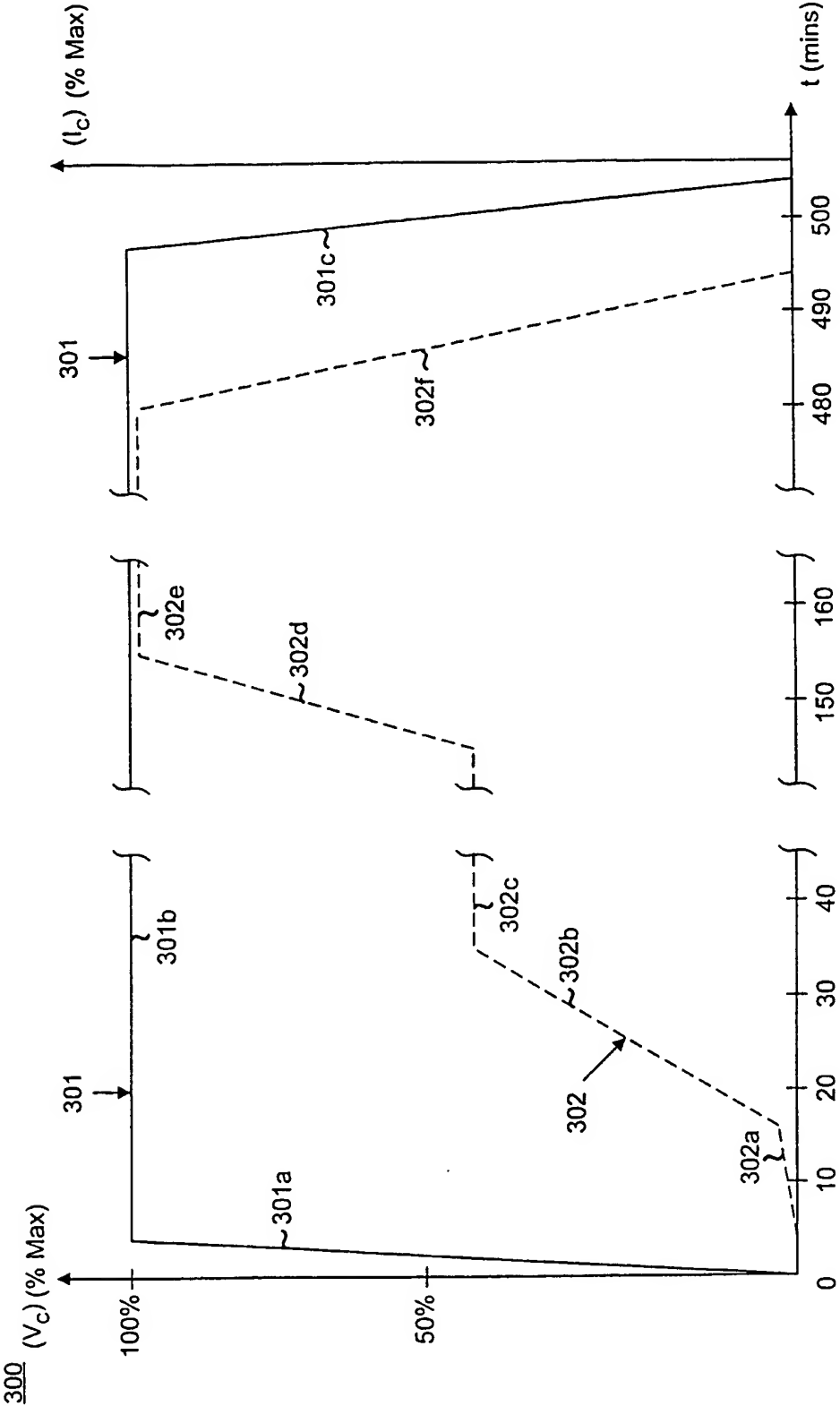


FIG. 3

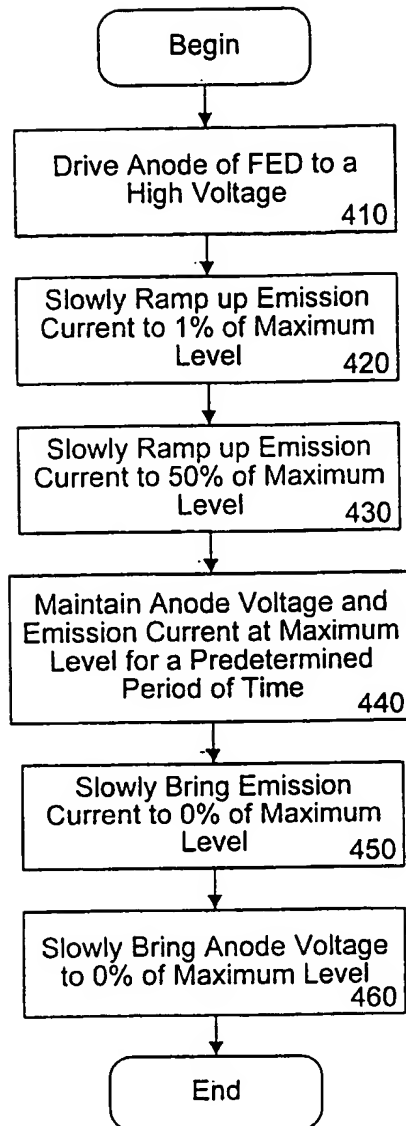
400

FIG. 4

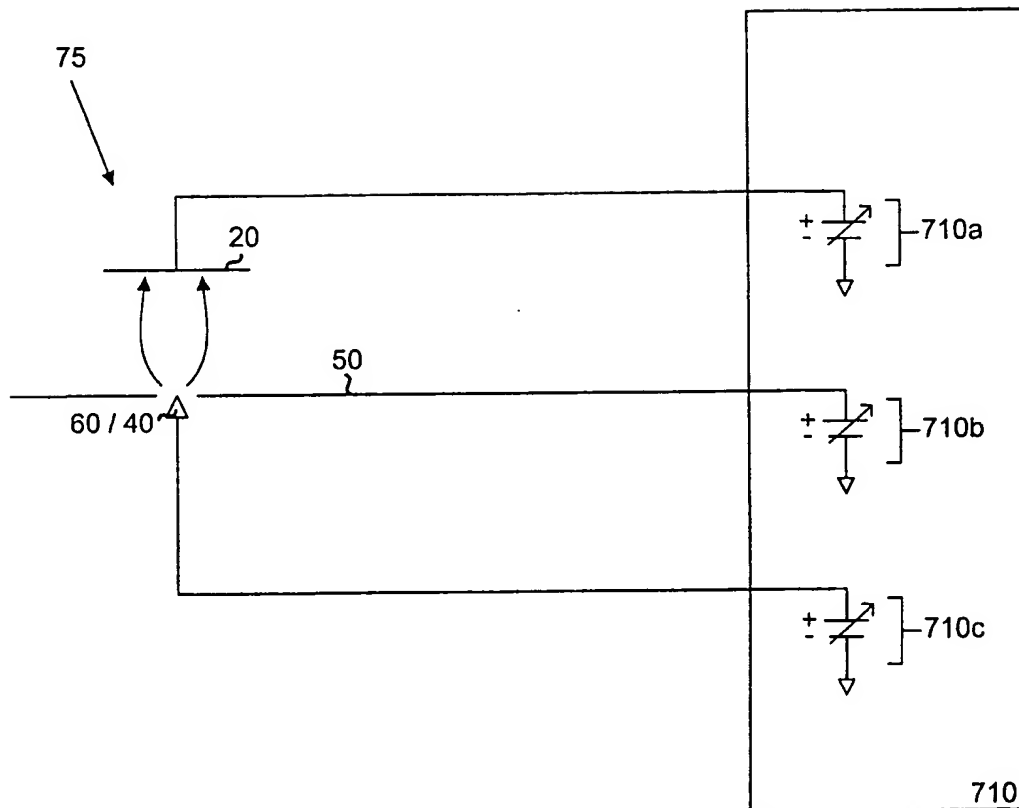
700

FIG. 5

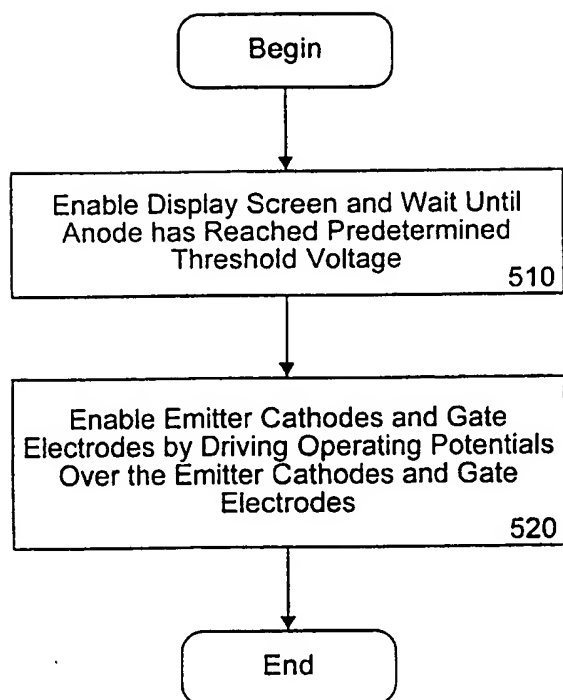
500

FIG. 6

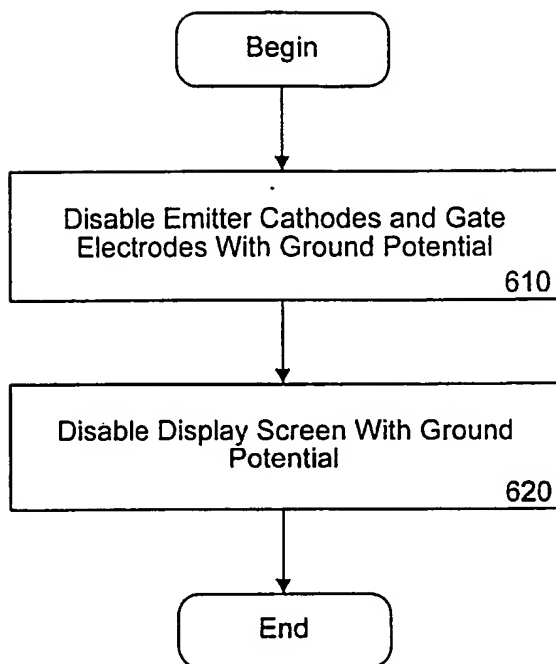
600

FIG. 7

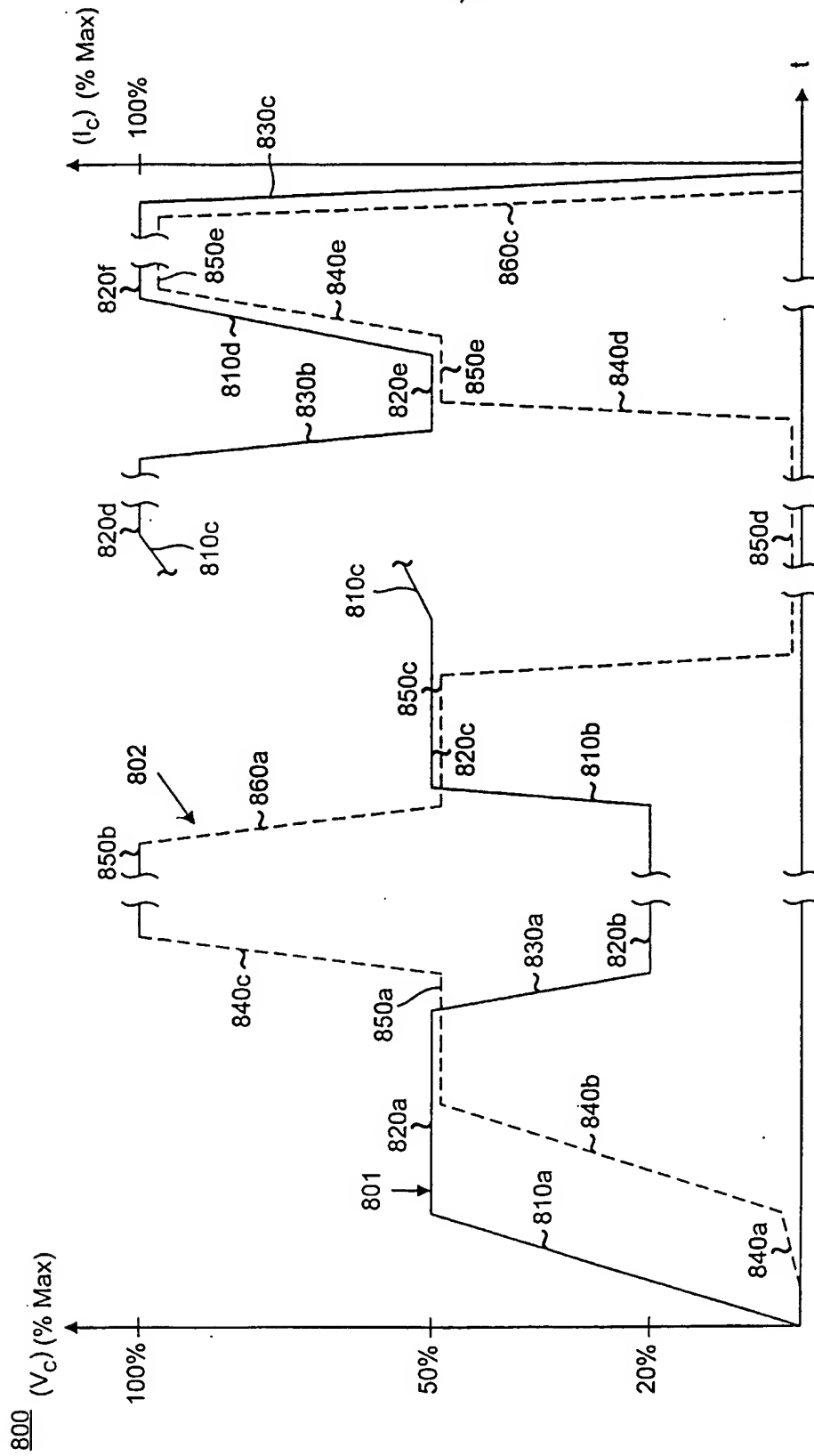


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/15588

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G09G 3/10

US CL :315/169.1, 169.3, 168; 313/495

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 315/169.1, 169.3, 168, 167, 160, 337; 313/495; 345/74, 75, 55, 214, 215

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,721,560 A (CATHEY, Jr. et al) 24 February 1998 (24/02/98), see entire document.	1-25
X	US 5,923,948 A (CATHEY, Jr.) 13 July 1999 (13/07/99), see entire document.	1-25
X	US 5,866,979 A (CATHEY, Jr. et al) 02 February 1999 (02/02/99), see entire document.	1-25
X	US 5,910,791 A (ZIMLICH et al) 08 June 1999 (08/06/99), see entire document.	1-25
X	US 5,898,415 A (HANSEN et al) 27 April 1999 (27/04/99), see entire document.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

25 OCTOBER 1999

Date of mailing of the international search report

18 November 1999 (18.11.99)

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703) 305-7724

Authorized officer

HAISSA PHILOGENE

Telephone No. (703) 305-3485